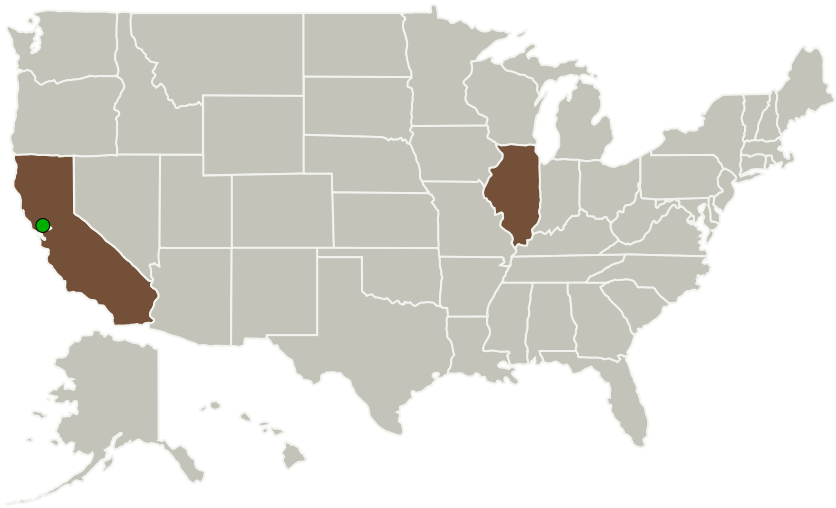
Scalable Parallel Algorithms for Formal Verification of Software, Phase I

Completed Technology Project (2012 - 2012)

Project Introduction

We will develop a prototype of a GPU-based parallel Binary Decision Diagram (BDD) software package. BDDs are a data structure that satisfies some simple restrictions, resulting in a unique representation of a Boolean function regardless of its actual implementation. This property of BDDs allows the efficient solution of many problems. The proposed tool will exploit multi-core CPUs and the thousands of stream cores in the latest graphics processors (GPUs) , which were made accessible to programmers through specialized software development kits. These large numbers of stream cores in GPUs, and the possibility to execute non-graphics computations on them, open unprecedented levels of parallelism at a very low cost. In the last 8 years, GPUs had an increasing performance advantage of an order of magnitude relative to x86 CPUs. Furthermore, this performance advantage will continue to increase in the next 20 years because of the scalability of the chip manufacturing processes. The technical objectives will be to efficiently exploit the GPU parallelism in order to accelerate the execution of a BDD package, and to explore hybrid approaches that will combine this GPU-based BDD package with our GPU-based parallel SAT solver that we are currently developing in a NASA SBIR Phase II project. The goal will be to achieve increased speed, as well as scalability for much larger state spaces when formally verifying complex software for space applications. We anticipate increase in both speed and scalability by 1 – 2 orders of magnitude by the end of Phase I, and 3 – 4 orders of magnitude by the end of Phase II, compared to the current approaches.

Primary U.S. Work Locations and Key Partners



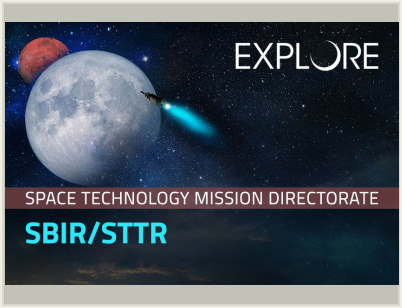


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Table of Contents

Small Business Innovation Research/Small Business Tech Transfer

Scalable Parallel Algorithms for Formal Verification of Software, Phase I

Completed Technology Project (2012 - 2012)

Organizations Performing Work	Role	Type	Location
Aries Design Automation, LLC	Lead Organization	Industry	Chicago, Illinois
Ames Research Center(ARC)	Supporting Organization	NASA Center	Moffett Field, California

Primary U.S. Work Locations	
California	Illinois

Project Transitions

February 2012: Project Start

August 2012: Closed out

Closeout Documentation:

- Final Summary Chart*(https://techport.nasa.gov/file/138479)*

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

Aries Design Automation, LLC

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

Carlos Torrez

Principal Investigator:

Miroslav N Velev

Co-Investigator:

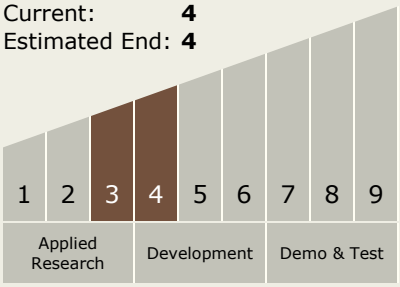
Miroslav Velev

Scalable Parallel Algorithms for Formal Verification of Software, Phase I

Completed Technology Project (2012 - 2012)

Technology Maturity (TRL)

Start: **3**
Current: **4**
Estimated End: **4**



Technology Areas

Primary:

- TX11 Software, Modeling, Simulation, and Information Processing
  - TX11.1 Software Development, Engineering, and Integrity
    - TX11.1.2 Verification and Validation of Software systems

Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System